# DIVISIONAL

# APPLICATION DATA SHEET

# FOR

# UNITED STATES LETTERS PATENT

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| APPLICANT NAMES: | K. Paul Muller<br>Hon-Sum P. Wong |
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| DOCKET NO.: | YO999-247DIV |
| ASSIGNEE NAME: | INTERNATIONAL BUSINESS MACHINES CORPORATION |
| ASSIGNEE RESIDENCE: | Armonk, New York |

# LATERAL PATTERNING

## BACKGROUND OF THE INVENTION

### *Field of the Invention*

The present invention generally relates to the formation of self-aligned structures in integrated circuit devices and more particularly to generating a lateral mask followed by lateral etching, deposition, diffusion or epitaxy.

### *Description of the Related Art*

Spacers are broadly used in the conventional formation of integrated circuit devices. The spacers are self-aligned structures generated laterally adjacent to an existing structure. The spacers can be used as a mask for vertical processing (e.g., as etch masks or implant masks).

However, conventional processing is limited to the formation of vertical features/structures self-aligned with the spacers. This limits the designers ability to form structures laterally. The invention overcomes this problem as discussed below.

## SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a structure and method for forming an integrated circuit chip having at least one opening in a substrate which includes forming an opening having vertical walls in the substrate, protecting a first portion of the vertical walls of the opening, leaving a second portion of the vertical walls unprotected, and laterally processing the second portion of the opening to change the shape of the opening. The laterally processing can include an isotropic wet etch, an isotropic dry etch or an anisotropic wet etch, selective deposition processes, selective epitaxial processes, or diffusion. The protecting includes forming a mask over the first portion of the vertical walls. The first portion can be the upper or lower portion of the opening. The first portion and the second portion can be alternating portions along a depth of the opening.

A second embodiment of the invention is a structure and method of forming an integrated circuit chip having at least one opening in a substrate which includes forming an opening having vertical walls in the substrate, protecting a first portion of the vertical walls of the opening, leaving a second portion of the vertical walls unprotected, and laterally patterning the second portion of the opening to form a step in the opening.

A third embodiment of the invention is a method of forming an integrated circuit chip having at least one transistor which includes forming an opening having vertical walls in a semiconductor substrate, protecting a first portion of the

vertical walls of the opening, leaving a second portion of the vertical walls unprotected, laterally patterning the second portion of the opening to form a step in the opening, and doping selected portions of the step to form two conductive regions separated by a semiconductive region. In the presence of an adjacent voltage field, the semiconductive region changes its conductivity and performs a switching operation in combination with the conductive regions.

Yet another embodiment of the invention is a method of forming an integrated circuit chip having at least one opening in a substrate which includes forming an opening having vertical walls in the substrate, protecting first portions of the vertical walls of the opening, leaving second portions of the vertical walls unprotected, wherein the first portions alternate with the second portions, and laterally etching the second portions of the opening to change a shape or property of the opening.

A further embodiment is an integrated circuit having at least one trench capacitor where the trench capacitor includes an opening having vertical sides, the vertical sides including a plurality of lateral openings, an insulator lining the opening and a conductor filling the opening. The lateral openings can be rectangular, v-shaped or curved openings in cross-section. The lateral openings increase a surface area and capacitance of the trench capacitor.

The invention is superior to conventional formation techniques because it allows for self-aligned patterning in the third dimension (i.e., laterally). Also, the size of the structures can be easily adjusted by altering of the depth of the

sacrificial and/or mask material, as discussed above. The depositions of the masking and sacrificial materials can be controlled much more precisely with the invention than with conventional lithographic techniques. This is especially true when the dimensions of the structures decrease.

## BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of preferred embodiments of the invention with reference to the drawings, in which:

Figure 1 is a schematic diagram of a partially formed structure according to the invention;

Figure 2 is a schematic diagram of a partially formed structure according to the invention;

Figure 3 is a schematic diagram of a partially formed structure according to the invention;

Figure 4A is a schematic diagram of a structure according to the invention;

Figure 4B is a schematic diagram of a partially vertical transistor;

Figure 5 is a schematic diagram of a partially formed structure according to the invention;

Figure 6 is a schematic diagram of a partially formed structure according to the invention;

Figure 7 is a schematic diagram of a partially formed structure according to the invention;

Figure 8 is a schematic diagram of a partially formed structure according to the invention;

Figure 9 is a schematic diagram of a partially formed structure according to the invention;

Figure 10 is a schematic diagram of a structure according to the invention;

Figure 11 is a schematic diagram of a partially formed structure according to the invention;

Figure 12A is a schematic diagram of a partially formed structure according to the invention;

Figure 12B is a schematic diagram of a partially formed structure according to the invention;

Figure 12C is a schematic diagram of a partially formed structure according to the invention;

Figure 13A is a schematic diagram of a deep trench capacitor structure according to the invention;

Figure 13B is a schematic diagram of a deep trench capacitor structure according to the invention;

Figure 13C is a schematic diagram of a deep trench capacitor structure according to the invention;

Figure 14 is a schematic diagram of the beginning of generation of vertical transistors according to the invention;

Figure 15 is a schematic diagram of the next step in generation of vertical transistors according to the invention;

Figure 16 is a schematic diagram of another step of generation of vertical transistors according to the invention;

Figure 17 is a schematic diagram of the next stage of generation of vertical transistors according to the invention;

Figure 18 is a schematic diagram of yet another stage of generation of vertical transistors according to the invention;

Figure 19 is a schematic diagram of the next phase of generation of vertical transistors according to the invention;

Figure 19 is a schematic diagram of another phase of generation of vertical transistors according to the invention;

Figure 20 is a schematic diagram of the finished devices after generation of vertical transistors according to the invention;

Figure 21 is another schematic diagram of the finished devices;

Figure 22 is a schematic diagram of the first stage in the formation of a silicon bridge for a bridge device according to the invention;

Figure 23 is a schematic diagram of the second stage in the formation of a silicon bridge;

Figure 24 is a schematic diagram of the formation of a silicon bridge during lateral patterning according to the invention;

Figure 25 is a schematic diagram of the formation of a silicon bridge after lateral patterning according to the invention;

Figure 26 is a schematic diagram of the free-standing silicon bridge device; and

Figure 27 is a flow diagram illustrating a preferred method of the invention.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

Referring now to the drawings, and more particularly to Figures 1-4, an embodiment of the invention is illustrated. Figure 1 illustrates a substrate 10 which can be a conductor, insulator or semiconductor. In a preferred example, the substrate 10 is a mono-crystalline silicon insulator. An opening 11 is formed in the substrate 10 using any of a wide variety of conventional methods, such as masking and etching processes.

Figure 2 illustrates a masking material 20 formed on the horizontal surfaces of the substrate 10. The masking material can comprise any conventional masking substance (such as an oxide, nitride, etc.). The masking material 20 can be deposited to be formed only on the horizontal surfaces of the substrate 10

using, for example, a mixture of silane, oxygen and argon gases in a high density plasma reactor.

In Figure 3, the inventive lateral patterning process is performed. This process involves an isotropic wet or dry etch or an anisotropic wet etch. The chemical composition of the etching solution used can comprise any conventional etching agent, such as $H_3PO_4$ for an isotropic etch of $Si_3N_4$, F (from $NF_3$) for an isotropic etch of Si in a chemical dry etch, and is preferably $NH_4OH$ for an anisotropic etch of Si. This process selectively removes material from the vertical surfaces (e.g., 110) of the substrate 10 as shown by the arrows 30 in Figure 3. Selectivities of several hundreds to one are possible.

The masking material 20 is then removed using a selective solution which dissolves the mask material 20 but does not affect the substrate material 10. The selective solution can comprise any conventional dissolving solution, such as a HF containing solution and preferably comprises 40:1 diluted HF.

The remaining structure, shown in Figure 4A, includes a step 40 which can be advantageously used in subsequent processing to form structures such as a partially vertical transistor, as shown in Figure 4B. More specifically, Figure 4B illustrates regions 44, 45 of the step 40 which have been doped to have a conductive state. The partially vertical transistor could be formed in a semiconductive substrate. Therefore, the region 46 would comprise semiconductor material. In operation, one electrical contact 41 would be connected to another electrical contact 42 by the application of voltage to a gate

conductor region 43 adjacent the semiconductor 46. The voltage in the gate conductor region 43 would change the conductivity of the semiconductor region 46 from conductive to non-conductive or, alternatively, from non-conductive to conductive, to perform a switching operation.

Figures 5-8 illustrate a second embodiment of the invention. More specifically, beginning with the structure shown in Figure 2, spacers 50 are formed as shown in Figure 5. The spacers can comprise any conventional material and are preferably formed of a material which can be selectively removed with respect to the substrate 10 and the mask 20. For example, the spacers can comprise SiN or polysilicon and are preferably formed of SiN. The spacers are generally formed by depositing the spacer material and subsequently removing the spacer material from horizontal surfaces using an anisotropic reactive ion etching (RIE) process which allows the material to remain only on vertical surfaces, thereby creating the spacers 50.

A portion of the mask 20 within the opening 11 is removed as shown by item 60 in Figure 6. This process also removes the mask 20 from other horizontal surfaces, except those areas protected by the spacers 50. For example, a reactive ion etch (RIE) which is selective to the mask material 20 (e.g., $CHF_3$, $CF_4$, $C_4F_8$, $O_2$, etc.) can be used to remove the mask material 20, without affecting the substrate 10, as shown in Figure 6. The spacers 50 can then be removed and the substrate 10 can be etched further as shown by item 70 in Figure 7 to extend the opening 60 below the level of the lowermost mask 20. Once again, a selective

reactive ion etching process (e.g., $NF_2$, HBr, or $O_2$) can be used to form the opening 70 without damaging the masks 20.

As shown in Figure 8, the inventive lateral patterning process (discussed above) is used to form the openings 80, 81. The masks 20 can then be removed. The remaining structure is especially useful in low resistance buried bit-line formations and other similar applications.

An alternative to the previous embodiment is shown in Figures 9-10. More specifically, in Figure 9, a sacrificial material 91 (e.g., boro-silicate glass (BSG)) 91 and a mask 92 (e.g., tetraethylorthosilicate (TEOS)) are deposited in an opening 90 in the silicon 10. Then an opening 93 is formed in the mask 92, using conventional methods, such as those discussed above. The mask 92 stays in place during selective removal of the sacrificial material 91 from the bottom of the trench and the inventive lateral patterning process forms the opening 100 to complete a bottle shape for a bottle shaped capacitor storage trench shown in Figure 10. After the opening 100 is formed, a node dielectric is formed by conventional means and the innear electrode is formed by conventional means. The structure is very useful for the subsequent formation of self-aligned bottle trench capacitor cells for DRAMs and other similar devices.

An important feature is that the upper portion 94 of the bottle opening 100 and the lower portion 95 of the bottle opening 100 are self-aligned by the inventive process. Further, the depth of the larger portion of the "bottle" is

determined by the depth of the sacrificial material 91 within the opening 90, which is easily controlled by conventional deposition processing.

Another embodiment of the invention is shown in Figures 11-13C. In Figure 11, the opening 11 within the substrate is filled with alternating layers of the mask material 20 and a sacrificial material 110 such as the boron silicate glass (BSG) mentioned above. More specifically, a small amount of the mask material 20 is deposited in the bottom of the opening 11, then a small amount of the sacrificial material 110 is deposited, then more of the mask material 20 followed by more of the sacrificial material 110 is deposited and the process is continued until the opening 11 is filled with alternating layers of mask material 20 and sacrificial material 110.

Then, an opening 111 is formed through the alternating layers and into the substrate 10 below the bottom most layer of mask material 20 (as indicated by item 112). The opening 111 is smaller than the opening 11 to allow the alternating layers to remain on the side walls of the opening 11. The sacrificial material 110 is then removed and the inventive lateral patterning process is used to create the lateral openings 120, as shown in Figure 12A.

In Figure 12A an isotopic etch is utilized to form the lateral openings 120 which are rectangular in cross-section. The openings 120 are rectangular in cross-section because the structure is aligned with the <111> plane. To the contrary, the same isotopic etching produces the V-shaped openings 121 shown in Figure 12B when the structure is aligned in the <100> plane. Figure 12C illustrates another

embodiment utilizing anisotopic etching which produces rounded lateral openings 122.

The structures shown in the Figures 12A, 12B, and 12C are extremely useful in forming deep trench devices that have increased capacitance. More specifically, as shown in Figures 13A, 13B, and 13C, the opening 111, 120-122 is lined with a thin insulator (e.g., an oxide or nitride) layer 130 as the dielectric of the capacitor and the remainder of the opening 111 is filled with a conductor 130 (e.g., metal, alloy, polysilicon, etc.) using well known conventional processes to form the inner electrode.

The structures formed according to the invention are superior to conventional structures. For example, the deep trench capacitor shown in Figures 13A, 13B, and 13C have a substantially increased surface area between the insulator 130 and the conductor 131 which produces a dramatic increase in the capacitance of the capacitor. Further, the remaining structures which can be formed using the inventive lateral patterning systems disclosed herein are advantageous over conventional structures because the self alignment is to the bottom of the initial tench. That results in a more uniform capacitance distribution.

Figures 14-21 illustrate one example of using the invention to form pairs of vertical transistors. More specifically, Figure 14 illustrates an opening 140 in a substrate 10. In Figure 15, the opening 140 is filled with alternating layers of mask material 150, 152 and sacrificial material 151 formed as discussed above. In

Figure 16, an opening 160 is formed through the layers 150-512 and in Figure 17, the inventive lateral patterning process (e.g., the removal of the sacrificial material 151) produces an opening 171. The height of opening 171 is determined by the depth 153 of the layer of sacrificial material 151, as shown in Figure 15, which, again, is easily controlled by conventional deposition processes.

In addition, in Figure 17, a gate insulator 171 (e.g., oxide) can be formed along the sides of the opening. Then, in Figure 18, the opening 160 is filled with a conductor 180, such as polysilicon, metal, alloy, etc. In Figure 19, an opening 190 is formed to remove the conductor 180 from the center of the structure. This produces alternating layers of mask material 151, 152 and conductor 180. The mask material 151, 152 is then removed, as shown in Figure 20, and the source and drain regions 201 are doped, using conventional methods. For example, the source/drain regions could be doped n+ or p+, $1E_2O/cm^3$ or higher, by diffusion or other well known methods.

An important feature of this embodiment is that the height 200 of the conductor 180 is determined by the deposition parameters of the sacrificial material 151. More specifically, the height 153, shown in Figure 15 will control of the height 200 shown in Figure 20. Therefore, the size of the conductor 180 is very easily controlled with the invention by simply altering the deposition parameters of the sacrificial material 151, as shown in Figure 15.

In Figure 21, the shallow trench isolation regions (STI) 210 are formed, as is well known in the art, to complete the transistor structure. Therefore, as shown

in Figure 21, the above process produces pairs of vertical transistors which have dimensions that are tightly controlled by the easily adjusted deposition process of the alternating mask and sacrificial material layers 150-152 shown in Figure 15.

Figures 22-26 illustrate yet another example of how the invention can be used to improve the formation of electronic devices. More specifically, this embodiment forms a silicon trench which can be used, for example, to form a dual-gate transistor.

Figure 22 illustrates a substrate 220 (such as a silicon substrate), and an insulator 221, such as many of the insulators discussed above, and a patterned structure 222, such as a silicon structure. In Figure 23, a mask material 230 is formed along the horizontal surfaces using the processes described above. In Figure 24, the material 222 is laterally patterned as shown by arrows 240 using the processes described above. As shown in Figure 25 the lateral patterning process is continued to completely remove the exposed portion of the material 222. Then, as shown in Figure 26, the insulator 221 and the mask 230 are removed to allow a suspended bridge of the material 222 to remain. A gate insulator can be formed on the suspended bridge and a gate conductor can then be formed around the bridge and the remaining well known processing can be performed to complete the dual gate transistor.

Figure 27 is a flow diagram of an embodiment of the invention. Item 2700 illustrates the forming of an opening 11 in the substrate 10. Item 2701 illustrates protecting a first portion of the vertical walls (mask) of the opening 11. Item 2702

illustrates the lateral patterning of a second portion 30 of the opening 11, as shown in Figures 1-3.

The inventive lateral patterning process is described above with respect to a few selected examples. However, the invention is not limited to the examples discussed. Instead, as would be known by one ordinarily skilled in the art given this disclosure, the invention is applicable to patterning and forming any structure which is subjected to conventional masking and patterning. The invention is superior to conventional formation techniques because it allows for self-aligned patterning in the third dimension (i.e., laterally). Also, the size of the structures can be easily adjusted by altering of the depth of the sacrificial and/or mask material, as discussed above. The depositions of the masking and sacrificial materials can be controlled much more precisely with the invention than with conventional lithographic techniques. This is especially true when the dimensions of the structures decrease.

While conventional lithographic techniques are optically limited to certain minimum features sizes, the inventive technique does not utilize optically patterned masks and can, therefore, produce structures which are smaller than those that can be produced using lithographic methods. Self-alignment is key in all high density integrated circuits and the invention opens the route for three-dimensional integration, since it allows for vertical self-alignment.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.